What is claimed is:

1. A production method for a semiconductor device which includes a super junction structural portion provided on a semiconductor substrate of a first conductivity and including drift layers of the first conductivity and RESURF layers of a second conductivity different from the first conductivity, the drift layers and the RESURF layers being laterally arranged in alternate relation in a direction parallel to the semiconductor substrate, the production method comprising the steps of:

forming a semiconductor layer of the first conductivity on the semiconductor substrate;

forming a trench in the semiconductor layer, the trench penetrating through the semiconductor layer to reach the semiconductor substrate;

filling a filling material in a predetermined bottom portion of the trench, so that a filling material portion is provided in the bottom portion of the trench up to a predetermined upper surface position which is shallower than an interface between the semiconductor substrate and the semiconductor layer and a void is provided in an upper portion of the trench above the predetermined upper surface position; and

after the filling step, introducing an impurity of the second conductivity into a portion of the semiconductor

layer exposed to an interior side wall of the trench, whereby the RESURF layers of the second conductivity are each formed alongside the interior side wall of the trench and the drift layers are each defined by a portion of the semiconductor layer remaining intact.

2. A semiconductor device production method as set forth in claim 1, wherein

the filling step includes the steps of:

supplying the filling material into the trench up to a position which is shallower than the predetermined upper surface position; and

after the filling material supplying step, etching back the supplied filling material to the predetermined upper surface position.

3. A semiconductor device production method as set forth in claim 1 or 2, wherein

the filling step includes the step of filling silicon oxide as the filling material in the trench.

4. A semiconductor device production method as set forth in any of claims 1 to 3, further comprising the step of oxidizing an interior wall of the trench to form an oxide film before the filling step, wherein

the filling step includes the step of filling polysilicon as the filling material in the trench.

5. A semiconductor device production method as set

forth in any of claims 1 to 4, further comprising the step of filling the void provided in the upper portion of the trench with an upper filling material after the RESURF layer formation step.

6. A semiconductor device production method as set forth in any of claims 1 to 5, further comprising the steps of:

introducing an impurity of the second conductivity into a surface portion of the semiconductor layer to form a base region of the second conductivity in contact with the RESURF layer and the drift layer;

introducing an impurity of the first conductivity into a portion of the base region to form a source region of the first conductivity which is isolated from the drift layer and the RESURF layer by the other portion of the base region;

forming a gate insulation film opposed to a portion of the base region between the source region and the drift layer; and

forming a gate electrode opposed to the portion of the base region between the source region and the drift layer with the intervention of the gate insulation film.

7. A semiconductor device production method as set forth in any of claims 1 to 6, wherein

the RESURF layer formation step includes the steps

of:

implanting the impurity of the second conductivity into a surface portion of the semiconductor layer exposed to the interior side wall of the trench; and

performing a thermal diffusion process to heat the resulting semiconductor substrate after the implantation step for diffusing the implanted impurity into the semiconductor layer.

8. A semiconductor device, comprising:

a semiconductor substrate of a first conductivity;

a super junction structural portion provided on the semiconductor substrate and including drift layers of the first conductivity and RESURF layers of a second conductivity different from the first conductivity, the drift layers and the RESURF layers being laterally arranged in alternate relation in a direction parallel to the semiconductor substrate; and

filling material portions each provided in a predetermined bottom portion of a trench penetrating through the super junction structural portion to reach the semiconductor substrate, wherein

the RESURF layers are each provided alongside an interior side wall of the trench,

the drift layers each have an isolation region present between the RESURF layer and the semiconductor

substrate to prevent the RESURF layer from contacting the semiconductor substrate, and

the filling material portions each have an upper surface located at substantially the same depth as an interface between the isolation region and the RESURF layer as measured from a surface of the super junction structural portion.

9. A semiconductor device as set forth in claim 8, wherein the filling material portions each comprise a silicon oxide portion.

10. A semiconductor device as set forth in claim 8 or 9, wherein the filling material portions each comprise a polysilicon portion covered with silicon oxide.

11. A semiconductor device as set forth in any of claims 8 to 10, further comprising upper filling material portions each provided in an upper portion of the trench above the filling material portion.

12. A semiconductor device as set forth in any of claims 8 to 11, further comprising:

base regions of the second conductivity each provided in contact with the drift layer and the RESURF layer;

source regions of the first conductivity each provided in contact with the base region and isolated from the drift layer and the RESURF layer by the base region;

and

gate electrodes each provided in opposed relation to a portion of the base region between the source region and the drift layer with the intervention of a gate insulation film.